REMARKS

The present amendment is made in response to the first Official Action, identified as Paper No. 3, and dated January 9, 2002. In the Action, the Examiner has rejected claims 1-6, 9-13, and 16 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent 5,828,245 in view of U.S. Patent No. 5,818,212; and rejected claims 7, 8, 14, and 15 under 35 U.S.C. §103(a) as being unpatentable over the '245 patent in view of the '212 patent and U.S. Patent 5,519,656. Claims 1-4, 6-8, and 17-19 remain pending in the present application.

Before providing the reasons why the amended claims are patentably distinct over the prior art, the '245 patent must be explained as it is the primary reference relied upon by the Examiner in rejecting the original claims. In addition, the intent of the inventions behind the '245 patent and present application must also be explained and understood. The '245 patent teaches a circuit that is used to reduce current draw on the boost supply, and has absolutely nothing to do with limiting an inrush current as such a problem does not exist in the driver circuits to which it is applied. Consequently, the circuit taught in the '245 patent is truly in a non-analogous art than is the present invention as one designing an inrush current limiting circuit would not look to power conserving circuits which do not need to limit inrush current.

Whether prior art is analogous is determined by two criteria: (1) whether the art is from the same field of endeavor, regardless of the problem addressed, and (2) if the reference is not within the field of the inventor's endeavor, whether the reference still is reasonably pertinent to the particular problem with which the inventor is involved. Wang Laboratories, Inc. v. Toshiba Corporation, et al, 993 F.2d 858, 864, 26 U.S.P.Q.2d 1767

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(Fed. Cir., 1993) (holding that prior art related to memory circuits in which modules of varying sizes may be added or replaced is non-analogous to patent that teach compact memory modules). The '245 patent is undoubtedly not within the same field as endeavor as the presently claimed invention (the '245 patent dealing with how to conserve power in the pre-driver side of a half-bridge DMOS circuit, and the present invention being concerned with limiting the inrush current being applied to a bulk capacitive load). Hence, the question becomes whether the '245 patent is reasonably pertinent to the problem the inventors are trying to solve in the instant case. See, Wang, 933 F.2d at 864. In this regard, the '245 patent is not a reference that lends itself to solving the problem of limiting inrush current in a circuit having a bulk capacitive load, as it instead involves engineering problems not contemplated by the present invention, and vice-versa. See, Paragraphs 7 and 8 of Bullock Declaration submitted herewith.

To this end, the '245 patent teaches a circuit that reduces current draw in the pre-driver stage of the half bridge DMOS circuit by switching off the power to the amplifier stage after the transition of Vcap and Vgate is complete. Thus, the threshold detectors send an enable or disable signal to the amplifier concurrent with predetermined threshold conditions being sensed by the circuit. This control of power to the amplifier is the essence of the invention taught in the '245 patent. Importantly, the load on the circuit of the '245 patent is a high side driver that operates from a supply voltage that is higher than the supply voltage of the power device (which is an entirely different type of load and circuit than the present application teaches which has a bulk capacitive load with a drive voltage equal to the supply voltage); by controlling the current supplied thereto via an

amplifier that only draws power when the voltage to the capacitor drops below a predetermined threshold, the draw on the power source is conserved.

The present invention comprises a circuit that is used to limit the inrush current from the power source because ignoring it may cause damage to the load. To limit the inrush current, the present invention employs a ramped voltage to an amplifier that is used as a reference voltage and then compared to voltage at the load such that the gate voltage output from the amplifier through the transistor and to the bulk capacitor load is virtually always equal to the ramp voltage, thereby sending a constant current to the load. It is critical to the success of the present circuit that the amplifier always remains "on." To turn it "off" would defeat the entire purpose of the invention, i.e., limiting inrush current to the load. Hence, but for the type of load present in the application of the present invention, there would be absolutely no reason to employ the circuit that is the subject of the present invention, thereby once again, reiterating the point that the '245 is truly non-analogous as the sole point to its circuit is to turn off the amplifier in order to cease drawing from the power source and thereby conserve power.

Addressing now amended claim 1, it recites the following:

1.An inrush circuit for electronic devices having high input capacitance, said inrush circuit comprising:

a. means for providing a voltage ramp;

b. means defining an output voltage;

c. an operational amplifier circuit having a reference input, said operational amplifier circuit receiving said voltage ramp at said reference input and comparing a divided sample of said output voltage with the voltage ramp,

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said operational amplifier operating in a linear mode, whereby said output voltage approximates a multiple of the voltage ramp;

d. transistor means electronically connected to said operational amplifier circuit, said transistor means operating in linear mode during capacitor charging, and subsequently reaching a full-ON state; and

e. energy storage load means connected to said transistor means for receiving said full power supply after said transistor means reaches its said full-ON state.

Claim 1 as amended essentially differs from original claim 1 by deleting the "time delay means" and adding the "energy storage means" as the load. The present circuit would work without the time delay, but would simply oscillate a little at the load. Thus, the time delay is not a critical element, although it does improve the functionality of the circuit. It is critical to the application of the present invention, however, that the load be some sort of energy storage means, most typically a bulk capacitor. This differs both in function and structure from the load taught in the '245 patent which is simply a high side DC powered device, such as a brushless motor, which could be characterized as an inductive, instead of a capacitive load. One fundamental difference in dealing with these types of loads is that an inductive load stores energy as current (creating voltage spikes on current steps), and as voltage in the capacitive load (creating current spikes on voltage steps). Protecting supply or load circuits in each case is quite different in approach. While protecting against inductive voltage spikes is simply a matter of proper use of diode clamps, protecting against capacitive current spikes involves more careful design of active networks, such as the one claimed in the present application. The '245 patent

teaches nothing of limiting current spikes in a load. While reference is made in the '245 patent to control of slew rate, it is solely for the intent of controlling EMI rather than inrush current, which again, is a totally non-analogous problem.

Relative to the 35 U.S.C. §103(a) rejection, wherein the '245 patent was combined with the '212 patent to reject original claim 1, the Examiner was relying on the '212 patent's showing of a voltage divider as part of the feedback to an amplifier, indicating that it would be obvious for someone skilled in the art to take that voltage divider and substitute it for the direct load voltage feedback that is used in the '245 patent, thereby showing the invention originally recited in claim 1. This, however, is an incorrect application of 35 U.S.C. 103 and the test set forth in Graham v. John Deere. In addition, for the same reasons that the '245 patent is truly non-analogous prior art, the '212 patent is also non-analogous prior art to the present invention. See Bullock Declaration at Paragraphs 7 and 9.

As previously stated, because of the loads that are used in the applications of the '245 patent and the present application, the '245 patent's circuit has no need for a voltage divider as the feedback as that may affect the comparators used to enable/disable the amplifier. The reason why a sample of the output voltage is used in the present invention is to ensure that the FET is saturated; in other words it provides control over the FET. The '245 patent's circuit does not need to control a transistor in this manner, and therefore never use a voltage divider to provide the amplifier with a sample of the output voltage. Thus, the '245 patent "teaches away from" using a voltage divider in the feedback loop.

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In addition to the fact that it is not obvious to one skilled in the art to substitute a divider circuit into the circuit of the '245 patent, claim 1 as amended is further distinguished over the '245 patent by expressly reciting the energy storage means which serve as the load. As discussed above, the '245 patent does not use an energy storage means as its load because of the application in which it is used. The present invention, however, is only used in applications where the load is some sort of energy storage means, and most typically a bulk capacitor. Consequently, the circuit taught in the '245 patent is not an appropriate reference for use in an "obviousness type/combining of references" analysis.

In view of the foregoing amendments as supported by these accompanying remarks and supporting papers, the Examiner's reconsideration and allowance of the present application is respectfully requested.

If the Examiner feels an interview is necessary to expedite prosecution of the present application he is urged to contact the undersigned at (315) 471-3151.

Respectfully submitted,

Date: 4/9/02

By _____
George R. McGuire
Reg. No. 36,603

GRM/arm

HANCOCK & ESTABROOK, LLP
1500 MONY Tower I
PO Box 4976
Syracuse NY 13221-4976

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Ann R. Miller

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VERSION TO SHOW CHANGES MADE

1. An inrush circuit for electronic devices having high input capacitance, said inrush circuit comprising:

[time delay means for eliminating false action;]

a. means for providing a voltage ramp [, operatively connected to said time delay means];

b. means defining an output voltage;

c. an operational amplifier circuit having a reference input, said operational amplifier circuit receiving said voltage ramp at said reference input and comparing a divided sample of said output voltage with the voltage ramp, said operational amplifier operating in a linear mode, whereby said output voltage approximates a multiple of the voltage ramp;

d. transistor means electronically connected to said operational amplifier circuit, said transistor means operating in linear mode during capacitor charging, and subsequently reaching a full-ON state [, in order to convey full power supply capacity to a load during normal operation] ; and

e. energy storage load means connected to said transistor means for receiving a full power supply after said transistor means reaches its said full-ON state.

Please cancel claims 5 and 9 – 16, and add the following new claims:

--17. The inrush circuit of claim 1, further comprising time delay means connected to said means for providing a voltage ramp.

18. The inrush circuit of claim 17, wherein said time delay means reaches threshold in about 50 ms.

19. The inrush circuit of claim 1, wherein said energy storage load means is a bulk capacitor.--